wherein each of said conductive members is comprised of a conductive layer formed on the surface of said semiconductor chip extending from said first electrode to said second electrode or said insulation layer.

SEE APPENDIX FOR CHANGE MADE TO CLAIMS 8 AND 9

REMARKS

Claims 8 and 9 have been amended so as to correct a minor grammatical error (consistent with line 12 of claim 6). If the Examiner maintains the pending rejections, entrance of the amendment is respectfully requested in order to place the application in better form for appeal.

In order to expedite prosecution, Applicants' representative initiated a telephone interview with Mr. Lee. Applicants and Applicants' representative would like to thank Mr. Lee for his courtesy in conducting the interview and for his assistance in resolving issues. In view of the following remarks, it is respectfully submitted that the present application is in condition for allowance.

I. CLAIMS 3, 8 AND 12 ARE NOT ANTICIPATED BY SAKAMOTO ET AL.

Claims 3, 8 and 12 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Sakamoto et al.. This rejection is respectfully traversed for the following reasons.

The Examiner alleges that "the depression formed in the solder ball by lead (306) ... clearly suggests that the lead (306) have elasticity for clamping object (300)" (*see* page 8, section 10, lines 5-8 of the outstanding Office Action). As is well known in patent law, a reference is

anticipatory only if each of the claim limitations are ***necessarily*** disclosed or suggested, rather than possibly disclosed. In the instant case, it is respectfully submitted that, at best, the lead 306 may possibly function as a clamp; but for the reasons that follow, it is submitted that lead 306 probably does ***not*** function as a clamp, let alone necessarily function as a clamp.

The dictionary definition of clamp is as follows:

> a device designed to press two or more parts together so as to hold them firmly (Merriam-Webster's).

It is respectfully submitted that the lead 306 does NOT necessarily "press [the opposing terminals 310] together so as to hold them firmly." It is submitted that a clamp must be configured to ***affirmatively*** press two elements together, rather than have an incidental resistive force. That is, a clamp has an intrinsic biasing force for holding two parts firmly together. Sakamoto et al. is completely silent as to the lead wire 306 having an intrinsic biasing force. Further, the depressions formed in the solder 308 can simply be, and likely are, the result of ***manually*** pressing the opposing ends of the U-shaped lead together when manufacturing the device. Once bonded, the lead 306 is kept in place by the ***adhesive property of the solder*** and NOT any clamping force of the lead. Accordingly, such depressions do NOT evidence that the lead 306 itself is ***necessarily*** a clamping device. For example, if a piece of loose string was bonded to the terminals 310 by pressing them into the solder 308, a depression would be made in the solder but the string is clearly NOT a clamp device (i.e., a string is not "***designed*** to ***press*** two or more parts together so as to hold them ***firmly*** together). Similarly to a piece of loose string, lead 306 can be a malleable metal which is forced into the solder but does not itself necessarily have an inherent biasing force "***designed*** to ***press*** two parts together ... etc".

Moreover, in Sakamoto, leads are formed on a connecting terminal so that the chip electrodes are not directly connected. In addition, leads and pads are formed only on one side of

the semiconductor package 300, whereas force is exerted from the other side via load generating device 330.

In contrast, the present invention can provide leads which are formed on two or more sides of the chip 1. Further, the connection can be completed by soldering, for example, rather than needing force.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently, in a single prior art reference, Akzo N.V. v. U.S. Int'l Trade Commission, 808 F.2d 1471 (Fed. Cir. 1986), and because Sakamoto et al. does not ***necessarily*** disclose, *inter alia*, a "conductive clip having elasticity for clamping objects", it is submitted that Sakamoto et al. does not anticipate claims 3, 8 and 12.

In addition, claim 8 further recites in pertinent part that "said semiconductor device units are stacked on each other, and said conductive members are connected to each other" (*see, e.g.*, Figure 8 of Applicants' drawings). In contrast, as clearly shown in Figure 5, the alleged semiconductor units 300 are adjacently positioned at the same level and are NOT stacked; and the alleged conductive members 306 are entirely spaced apart and not connected to each other.

Based on the foregoing, it is submitted that claims 3, 8 and 12 are patentable over Sakamoto et al.. Accordingly, it is respectfully requested that the rejection of claims 3, 8 and 12 under 35 U.S.C. § 102(e) over Sakamoto et al., be withdrawn.

II. CLAIM 6 IS NOT ANTICIPATED BY GAYNES ET AL.

Claim 6 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Gaynes et al.. This rejection is respectfully traversed for the following reasons. During the interview with Mr.

Lee, it was tentatively agreed that Gaynes et al. does not anticipate claim 6 for the reasons that follow.

A. The Examiner relies on element 85 shown in Figures 8A, B of Gaynes et al. as the recited "semiconductor chip." However, none of the individual semiconductor chips 85 have a first electrode formed on the first major surface of the semiconductor chip and a second electrode (and/or insulation layer) ***formed on the opposing second major surface of the same semiconductor chip*** as recited in claim 6 (*see, e.g.,* Figure 7 of Applicants' drawings). In contrast, each of the semiconductor chips 85 have metallizations formed on ***only one side*** thereof (*see* col. 10, line 57). Accordingly, it is submitted that Gaynes et al. does not disclose the ***combination*** of stacked semiconductor device units, whereby the individual semiconductor chip forming part of the semiconductor device unit has an electrode on both sides thereof.

B. Further, Gaynes et al. does not disclose or suggest, "wherein a first chip has a first conducting pattern extended from said first electrode, a second chip has a second conducting pattern extended from said second electrodes, and a bump is provided between said first conducting pattern and said second conducting pattern, which face to each other, for electrically connecting said two conducting patterns." The Examiner simply refers to Figures 8A,B for allegedly disclosing these features.

However, it is submitted that Gaynes et al. is completely silent as to conducting patterns that extend from electrodes. Although wires 84 may potentially be connected to electrodes (not shown in the drawings), this conclusion does NOT necessitate that the electrodes themselves have conducting patterns extending therefrom (*compare, e.g.,* Figure 6 of Applicants' drawings which shows electrodes 2 but not a conducting pattern, whereas Figure 7 discloses conducting patterns 2a,3a extending from electrodes 2,3). In fact, as shown in Figure 8A,B, the wires 84 do

not appear to be connected to anything but the surface of the chips 85. Even assuming that they are connected to electrodes, however, the bare surfaces of the chips 85 indicate that no other conducting patterns exist, let alone ***extending from*** the electrodes.

Moreover, even further assuming *arguendo* that there are conducting patterns on the surface of the chips 85 AND that they extend from the electrodes, this conclusion does NOT necessitate that the alleged bump 81 is provided ***between*** conductive patterns which face each other from opposing chips. For example, bump 81 can simply be positioned between the alleged electrodes.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently, in a single prior art reference, Akzo N.V. v. U.S. Int'l Trade Commission, 808 F.2d 1471 (Fed. Cir. 1986), and because Gaynes et al. does not disclose or suggest, *inter alia*, "a semiconductor chip" having an electrode on both sides thereof while forming part of a stacked semiconductor device unit, and also does not disclose conductive patterns extending from the electrodes (let alone with a bump therebetween), it is submitted that Gaynes et al. does not anticipate claim 6.

Based on the foregoing, it is submitted that claim 6 is patentable over Gaynes et al.. Accordingly, it is respectfully requested that the rejection of claim 6 under 35 U.S.C. § 102(e) over Gaynes et al., be withdrawn.

III. CLAIMS 4, 9 AND 13 ARE PATENTABLE OVER SAKAMOTO ET AL. IN VIEW OF WHITNEY ET AL.

Claims 4, 9 and 13 stand rejected under 35 U.S.C. § 103 over Sakamoto et al. in view of Whitney et al.. This rejection is respectfully traversed for the following reasons. During the

interview, Mr. Lee indicated that he understood why Applicants believe the proposed combination is improper but requested that the relevant arguments be made of record.

The Examiner relies on col. 1, lines 26-31 of Whitney et al. for providing the motivation to make the proposed combination. In particular, the Examiner alleges that the proposed combination would be motivated for "the purpose of increasing reliability and operation of the package" (*see* page 8, lines 3-4 of the outstanding Office Action). However, for the reasons that follow, it is submitted that col. 1, lines 26-31 of Whitney et al. does not provide any motivation for using the conductive layer 70/80 in the device of Sakamoto et al.. In other words, it is submitted that the asserted benefits disclosed by Whitney et al. are NOT attributable to the device of Sakamoto et al..

Whitney et al. is directed to circuit protectors, and in particular, improving the contact area of a fuse element with electrical terminations (*see* col. 1, lines 19-25). As discussed in col. 1, Whitney et al. discloses that fuse elements require good contact with terminations so as to improve their reliability/operation. Accordingly, Whitney et al. discloses the end terminations 70/80 in order to "provide a greater contact area than previously known in the art for improving the electrical connection of the terminations to the fuse" (*see* col. 1, lines 49-55). The terminations 70/80 increase the contact area through connection to the fuse via the ***lateral/end edges*** of the substrate. It is therefore submitted that the motivation relied on by the Examiner is directed to improving the reliability/operability of a ***fuse element*** by increasing contact area between terminations and the fuse through ***end/lateral edges*** of the substrate. That is, the alleged motivation relied on by the Examiner for making the combination is for "increasing the reliability and operation" ***of a fuse element*** and is not relevant to the device of Sakamoto et al..

In particular, Sakamoto et al. is NOT a circuit protector and has no fuse element. In fact, Sakamoto et al. does not have any electrical connection on the end/lateral edges of the substrate (*see* Figure 5). Accordingly, placing the terminations 70/80 into the device of Sakamoto et al. would NOT increase "reliability and operation of the package" as alleged by the Examiner because the terminations 70/80 would not be ***electrically*** connected to the end/lateral edges of the substrate as is required in the device of Whitney et al. in relation to the fuse element. Without a fuse, Sakamoto et al. has no need or purpose to increase contact area between the lead and the end/lateral edges of the substrate.

The structural/functional differences between the devices of Sakamoto et al. and Whitney et al. further evidence the lack of motivation for making the proposed combination. Specifically, Whitney et al. does not have electrodes on ***opposing major surfaces*** of the chip as in the device of Sakamoto et al.. The terminations 70/80 are electrically connected only to the end/lateral edges of the substrate, and has no ***electrical*** connection with the opposing major surfaces of the chip.

In summary, the motivation derived from Whitney et al. relied on by the Examiner to make the proposed combination is ***specific to devices having fuses*** (to increase contact area with the fuse to improve reliability/operation) interconnected through ***lateral/end edges*** of the substrate; whereas Sakamoto et al. does not have any electrical connection at the lateral/end edges of the substrate, let alone a fuse element. As such, the Examiner's alleged motivation fails, rendering the proposed combination improper as being based solely on improper hindsight reasoning using only Applicants' specification as guide to reconstruct the claimed invention using bits and pieces of the prior art.

At best, the Examiner has attempted to show only that the elements of the claimed invention are ***individually*** known without providing a *prima facie* showing of obviousness that the ***combination*** of elements recited in the claims is known or suggested in the art. For all the foregoing reasons, it is submitted that the proposed combination of Sakamoto et al. in view of Whitney et al. is improper.

Based on the foregoing, it is submitted that claims 4, 9 and 13 are patentable over Sakamoto et al. in view of Whitney et al.. Furthermore, it is submitted that claim 9 is patentable for the additional reasons discussed above with respect to claim 8 (i.e., Sakamoto et al. does not disclose or suggest "said semiconductor device units [being] stacked on each other, and said conductive members [being] connected to each other." Accordingly, it is respectfully requested that the rejection of claims 4, 9 and 13 under 35 U.S.C. § 103 over Sakamoto et al. in view of Whitney et al., be withdrawn.

IV. CLAIMS 14-16 ARE NOT ANTICIPATED BY AKRAM ET AL. NOR SUGANI ET AL.

Claims 14-16 stand rejected under 35 U.S.C. § 102 as being anticipated by Akram et al. and Sugani et al.. This rejection is respectfully traversed for the following reasons.

In the previous response filed November 21, 2001, Applicants argued that neither Akram et al. nor Sugani et al. disclosed "***conductive patterns*** of said spacer members [that] are electrically connected to ***each other***" as recited in claim 14. In contrast, conductors 26 of Akram et al. are ***electrically isolated*** from each other as shown in Figure 3 of Akram et al. and conductors 312 of Sugano et al. are ***electrically isolated*** from each other as shown in Figure 48 of Sugano et al..

In response to this argument, the Examiner asserted that Akram et al. and Sugano et al. "clearly discloses that the ***electrodes*** [are] electrically connected to the conductive patterns" (*see* outstanding Office Action, page 10, lines 16-17 and page 11, lines 6-7). It is respectfully submitted that the Examiner's assertion is not relevant to Applicants' argument that the prior art does not disclose ***conductive patterns*** that are electrically connected to each other. That is, the Examiner's assertion is directed to the connection between the electrodes and the conductive patterns rather than the connection between the conductive patterns themselves.

Based on the foregoing, it is submitted that claims 14-16 are patentable over Akram et al. and Sugano et al.. Accordingly, it is respectfully requested that the rejection of claims 14-16 under 35 U.S.C. § 102 over Akram et al. and Sugano et al., be withdrawn.

V. CONCLUSION

Having fully and completely responded to the Office Action, Applicant submits that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

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APPENDIX

8. (Twice Amended) A semiconductor device comprising:

a plurality of semiconductor device units, each of said semiconductor device units including:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;

wherein said semiconductor device units are stacked on each other, and said conductive members are connected to each other,

wherein each of said conductive members is comprised of a conductive clip holding said first electrode together with said second electrode or said insulation layer, said conductive clip having elasticity for clamping objects.

9. (Twice Amended) A semiconductor device comprising:

a plurality of semiconductor device units, each of said semiconductor device units including:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;

wherein said semiconductor device units are stacked on each other, and said conductive members are connected to each other,

wherein each of said conductive members is comprised of a conductive layer formed on the surface of said semiconductor chip extending from said first electrode to said second electrode or said insulation layer.